A Conceptual 12-bit Column-Parallel Time-Domain Binary Search TDC-Interpolated Single-Slope ADC Architecture

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SUMMARY

* Goal: 12-bit 0.5 µs A/D conversion in 5 µm x 800 µm column-parallel form factor.

* Means: use a TDBS TDC interpolator in an SS ADC (Illustration 1-2).

* Unsolved Challenge: in-column reference delay element stability.

* Global drift issues solved partially through online self-calibration (Illustration 3).

*Delay mismatch and PSRR immunity still remains an issue and topic for further investigations (Illustration 4).

Illustration 1: Ramp Interpolation Mechanism

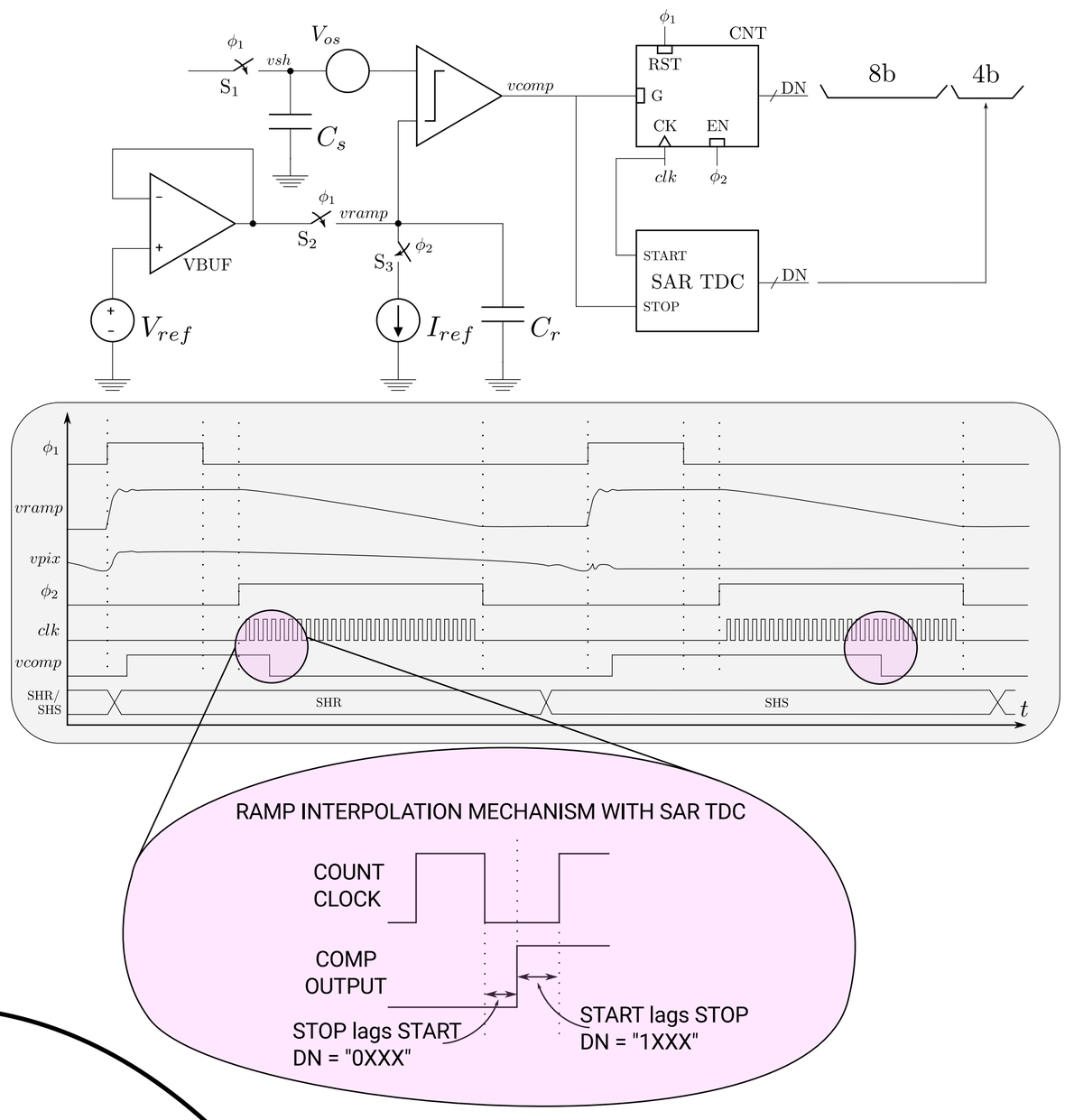


Illustration 2: TDBS Concept

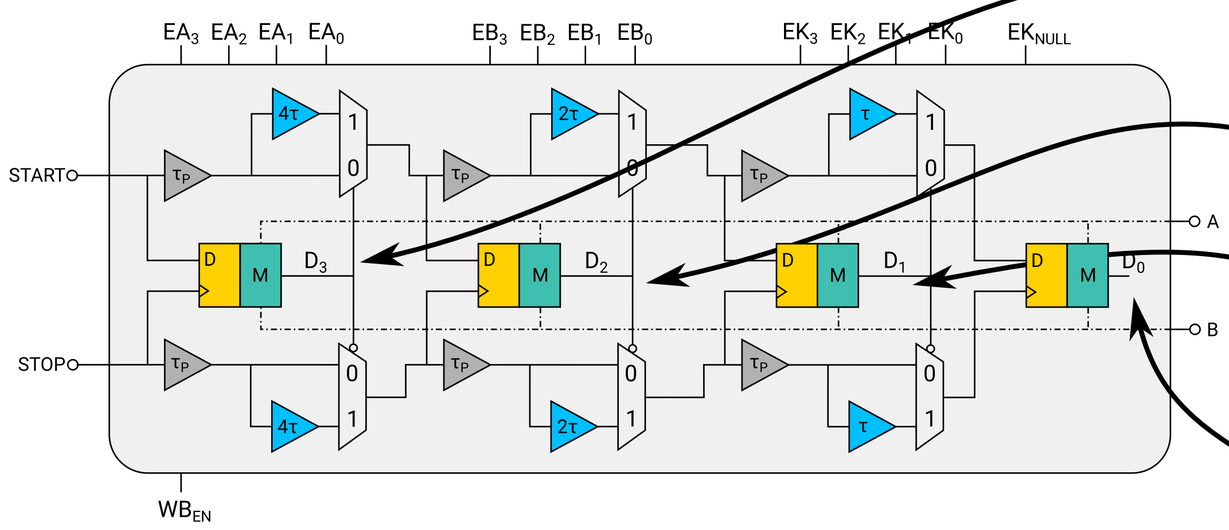
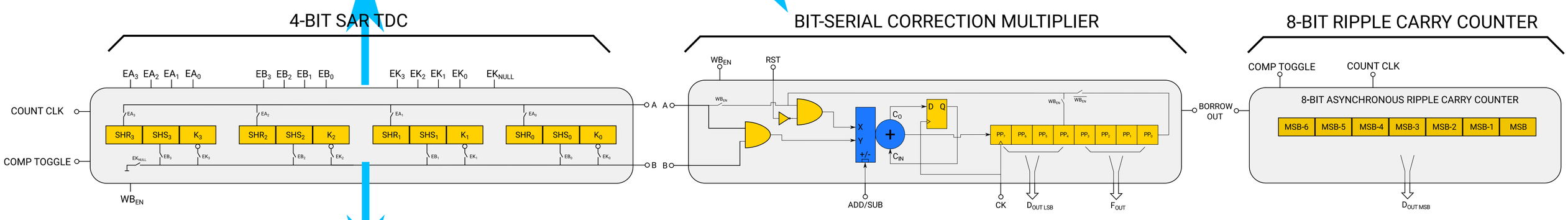


Illustration 3: x1 column ADC with correction

$$K = \frac{\text{IdealFullScale}}{\text{MeasuredFullScale}}$$

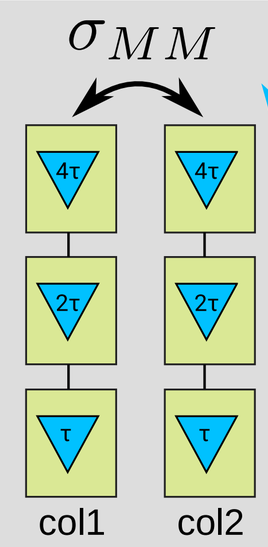


COEFFICIENT (K) TABLE

15/15 = 1	15/9 = 1.66	15/3 = 5.00
15/14 = 1.07	15/8 = 1.88	15/2 = 7.5
15/13 = 1.15	15/7 = 2.14	15/1 = 15
15/12 = 1.25	15/6 = 2.50	15/0 = ...
15/11 = 1.36	15/5 = 3.00	
15/10 = 1.50	15/4 = 3.75	

we want to operate in this range
minimizes numerical noise — delay
PVT corners designed to drift here

Illustration 4: challenge — delay mismatch and PSRR

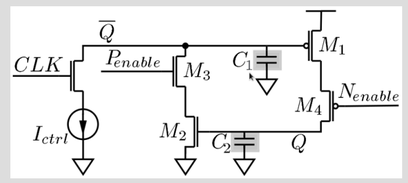


POSSIBLE DELAY MATCHING SOLUTIONS

matching for DNL <0.5
$\sigma_{MM} = \pm 1/4\tau$

* high TDC DR increases delay matching challenge — use fast clock
* investigate DEM technique applicatility
* randomize ADC pedestal

* use thyristor-based delay
* use lots of decoupling
* other MM-immune delays?
* e.g.:



A CMOS Thyristor Delay