**SUMMARY**

* **Goal:** 12-bit 0.5 μs A/D conversion in 5 μm x 800 μm column-parallel form factor.

* **Means:** use a TDBS TDC interpolator in an SS ADC (Illustration 1-2).

* **Unsolved Challenge:** in-column reference delay element stability.

* Global drift issues solved partially through online self-calibration (Illustration 3).

*Delay mismatch and PSRR immunity still remains an issue and topic for further investigations (Illustration 4).

**Illustration 2: TDBS Concept**

**Illustration 3: x1 column ADC with correction**

$$K = \frac{\text{IdealPullScale}}{\text{MeasuredPullScale}}$$

**Illustration 4: challenge — delay mismatch and PSRR**

$$\sigma_{MM} = \pm 1/4T$$

POSSIBLE DELAY MATCHING SOLUTIONS

- use thyristor-based delay
- use lots of decoupling
- other MM-immune delays?
- e.g.:

A CMOS Thyristor Delay

we want to operate in this range minimizes numerical noise — delay PVT corners designed to drift here

COEFFICIENT [K] TABLE

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<td>15/15 = 1</td>
<td>15/9 = 1.66</td>
<td>15/3 = 5.00</td>
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<tr>
<td>15/14 = 1.07</td>
<td>15/8 = 1.88</td>
<td>15/2 = 7.5</td>
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<tr>
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<td>15/7 = 2.14</td>
<td>15/1 = 15</td>
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<tr>
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<td>15/6 = 2.50</td>
<td>15/0 = ...</td>
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<tr>
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<td>15/10 = 1.50</td>
<td>15/4 = 3.75</td>
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**Illustration 1: Ramp Interpolation Mechanism**