Worst case resistor mismatch in an R-2R ladder DAC

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Before diving into practical simulations with normally distrubuted mismatch over a resistive DAC ladder to be designed, it is essential to estimate the resistor mismatch scenario when the worst case linearity would occur. In addition such an estimation, would give a better overview of the critical points of the system and would possibly hint the various ways of compensating such errors.

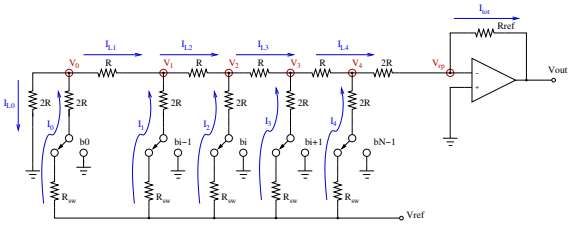

Figure 1: Current distribution in an R-2R DAC

If we consider the DAC shown on Figure 1 assuming that it is a 4-bit converter, ideally the INL should be within ±0.5 LSB, or in our case with $V_{ref} = 1.2$V that will be:

$$\frac{\frac{V_{ref}}{2^N}}{2} = \frac{\frac{1.2}{2^4}}{2} = 0.0375V \tag{1}$$

Following Kirchoff's Current Law (KCL) we can see that $I_{L0} + I_{L1} + I_{L2} + I_{L3} + I_{L4} = I_0 + I_1 + I_2 + I_3 = I_{tot}$, in addition the currents at nodes I_{0-3} and I_{L0-L3} will be equal to respectively (ignoring the R_{sw}):

$$I_{0\div 3} = \frac{V_{0\div 4}}{2R} \tag{2}$$

$$I_{L1\div L2} = \frac{V_{1\div 2} - V_{2\div 3}}{R} \tag{3}$$

$$I_{L0\&L3} = \frac{V_{ref\&3} - V_{0\&rp}}{2R} \tag{4}$$

The currents in the switch current paths will be:

$$I_0 = \frac{V_{ref} - V_0}{2R} \tag{5}$$

and respectively:

$$I_{L1\div L4} = \frac{V_0 \div V_{rp}}{R} \tag{6}$$

Following Equations 5 and 6 we can observe that if the ratio between the resistors (2R) in the I_{0-3} current paths and the resistors (R) in the I_{L1-L4} paths is impaired, and of course if this applies to all pairs, then a worst case INL will be observed. The transfer function in the aforementioned case will look like the one represented in Figure 2.

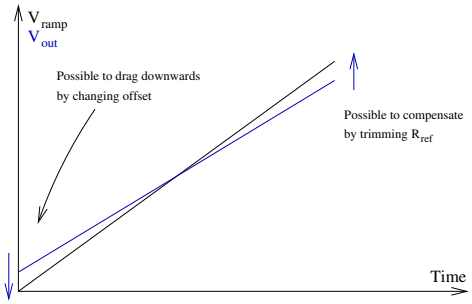

Figure 2: INL in the abovementioned 2R-R mismatch case and a way of compensating the errors from this case

However, the expression "worst case" is hard to be defined, due to the fact that the abovementioned case of worst INL can very easily be tuned if the amplifier's feedback (R_{ref}) can be trimmed and if a differential offset can be applied to the non-inverting input of the opamp. However there could be another case, which might be more difficult to cope with without having to trim the R-2R ladder. This is the case where every adjacent R-2R ladder sub-steps are mismatched by $\pm\sigma_{max}$, or to ease the visualisation Figure 3 represents the described mismatch case.

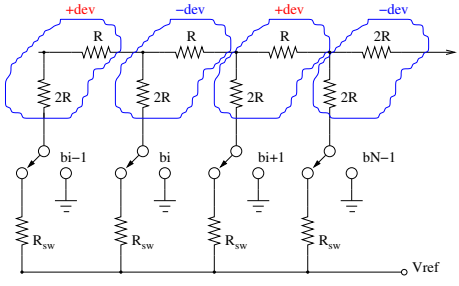

Figure 3: INL due to mismatch in adjacent sub-stages

Having such resistor mismatches between the adjacent sub-ladders (bits) will result in a non-linear transfer function and slope between different weight bits (example: "01111" and "10000"). While in the first case a voltage controlled gain of the amplifier and offsets are not difficult to realise, the second case will need additional circuitry for balancing each bit. Figure 4 shows the expected transfer function for the case with mismatched adjacent sub-stages.

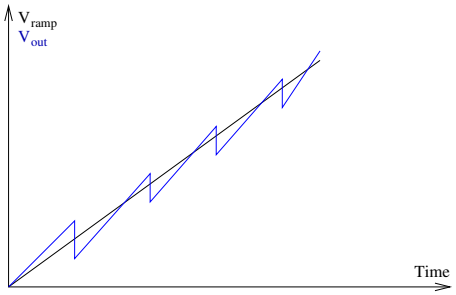

Figure 4: INL deviation due to mismatch in adjacent sub-stages

In reality there will be a complex mismatch over all resistor ratios, for which, depending on the use additional process resistor trimming or embedded architecture calibration techniques should be introduced. The following subsections will describe a resistor model and possible trial simulations to reproduce the aforementioned mismatch errors.

Resistor model

Apart from the corner cases, throughtout the development of a real converter (for tape-out) in many cases it is essential to be able to estimate how many chip units will meet the design specifications and how many will not, also called yield estimation. For these purposes, usually statistical value variation

component models are used provided by the factory.

There are various technical ways of modelling such variations. Practicly almost every SPICE-like simulator has statistical analysis capabilities, the Spectre simulator used here is among one of them. Following the reference guide from [1] the resistors were modelled in Spectre with 10% process variations and 0.5% mismatch by using the *process* and *mismatch* statistical environments, for generating gaussian distributed random resistor values, which are afterwards instantiated multiple times in our netlist. An example of the statistic block environment can be seen below:

```
section mm
  statistics{
   process {
   vary resp dist=gauss std=10 percent=yes
           }
   mismatch{
   vary resmm dist=gauss std=0.5 percent=yes
           }
  }
```

In addition, another way for resistor modelling the is the usage of VerilogA and the $RDIST_NORMAL function, providing normally distributed random numbers, which could be then multiplied by a coefficient to model the variations.

Modelling of the resistor's parasitic capacitance to the substrate can also be introduced. Lumping two capacitor additions to the two resistor nodes in the netlist connected to ground provides sufficient accuracy. The capacitor values can be estimated by taking the product of the sheet area capacitance coefficient and area of the resistor itself. For the performed test, roughly 150 fF/kΩ were introduced in total for both capacitors.

Process and mismatch variation Monte Carlo runs

A 1000 run Monte Carlo test was performed, by using the models described above. Some yield numbers were estimated to be roughty 88.1% for converters within INL lower than ±0.5 LSB and 94.7% within ±1 LSB. A distributon histogram of the resuts can be observed on Figure 5. All these numbers aim to show a possible procedure-flow of a potential mismatch and process variation analysis. The aforementioned numbers and graphical representations show theoretical results for the current setup.

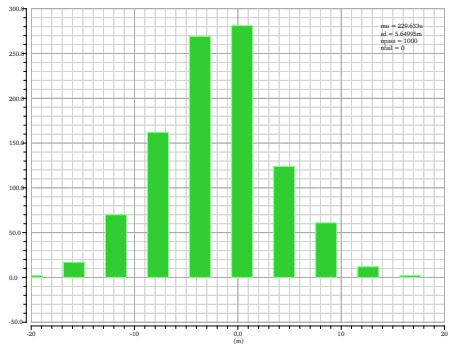

Figure 5: INL distribution for a 1000 run monte carlo test

As expected with random mismatch the DAC's transfer curve appears to be similar to the one predicted in Figure 4. Some highly exaggerated plots from the simulated converter confirming a variation of 10% can be observed on Figure 6. The most probable explanation of the glitches seen on the figure, could be due to the parasitic capacitance on the resistor ladder nodes, introducing a certain delay between the switching of adjacent bits, therefore resulting in a very short mo-

ment of current straying, resulting therefore into a voltage glitch. As the used amplifier model is ideal, with close to infinite gain, such glitching is not a surprise.

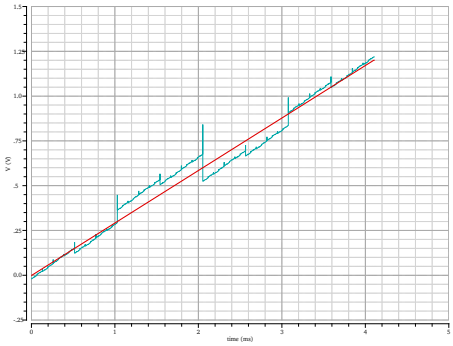

Figure 6: Mismatched DAC's ramp transfer function

It should be mentioned that apart from INL and DNL it is also essential to test mismatch effects (defects) in terms of dynamic parameters like SNR, SHNR, etc. This of course would require the addition of a shaping filter in the testbench and the very same calculator expressions using the SPECTRUM function for evaluating the SINAD, SFDR, SHNR etc. For regret due to some technical problems with the INL runs and their troubleshooting, the time assigned for these estimations, as well as a second pole model of the DAC's opamp have not been performed.

References

O'RIORDAN, DON *Recommended Spectre Monte Carlo Modeling Methodology.* The Designer's Guide Community, 2003